Amendments to the Specification:

Please replace the paragraph beginning at line 24, page 6, with the following:

Exposing ~~{of}~~ a large portion of silicon fin 114 allows for silicon to be selectively grown on ~~{this}~~ the exposed faces and improves the benefit achieved by a subsequent silicide and epitaxial process. Referring to FIGs 10 and 12, a selective epitaxial growth is performed to form additional conductive regions or source/drain epitaxial structures 150 shown in the cross section view of FIG 11 (from above). The thick source/drain epitaxial structures 150 reduce the source/drain resistivity and facilitate the subsequent formation of contacts or vias to the source drain regions. A silicide sequence is performed to silicide exposed portion of fins 114. In this sequence, an appropriate metal such as tantalum or titanium is non-selectively deposited over the wafer and subjected to a heat step. Wherever the metal contacts silicon, a silicide is formed during the heat step. The presence of confined spacers 144 prevents the silicide from forming on sidewalls of first layer portion 142 and thereby prevents the formation of an electrical path (short) between the gate electrode and the source/drain regions. By confining the gate structure sidewall spacers to the region in close proximity to the gate structure, the epitaxial structures 150 cover substantially all of the previously exposed portions of silicon fin 114.

Please replace the paragraph beginning at line 24, page 7, with the following:

After forming the silicon spacers 202 and capping layer 210, conventional lithography is used to form a gate mask photoresist pattern. Thereafter, a gate etch and trim process is performed to produce ~~{a formation}~~ a gate structure 221 as shown in FIGs 17 and 18. Gate structure 221 includes the remaining portions 220 of capping layer 210 and the remaining portions 212 of polysilicon spacers 202. The remaining spacer portions 212 are undercut with respect to capping layer portion 220 as shown in FIG 17. This undercutting result in voids 211 being formed adjacent the sidewalls of remaining spacer portions 212 under the overhanging capping layer. As shown in FIG 19, dielectric spacers 230 are formed where the voids 211 were present by depositing a dielectric such as silicon nitride and performing an anisotropic etch. Like the dielectric spacers 144 of FIG 10, dielectric spacers 230 are confined to the sidewalls of remaining (polysilicon) spacer portions 212, which serve as the gate electrode. The remaining portions of silicon fins 114 are exposed for subsequent silicide and selective epitaxial processing as described above with respect to FIGs 10 through 12.